Adjustable Low-Power Non-overlap Clock Generator for Switched-Capacitor Circuits

Melikyan Vazgen Sh., Galstyan Vache A., Melikyan Nazeli V., Aleksanyan Ani L. and Borisav Jovanović

***Abstract*— This paper presents design of energy-efficient non-overlap clock generator (NOCG) based on three transistor XOR gate. Two control voltages provide adjustable non-overlap period and assure 50% duty cycle of two phase output signal. The proposed structure is simple and uses less MOS transistors than in conventional NAND based NOCGs. Due to structure of XOR gate and controllable signal-to-ground resistance, small dynamic power consumption was achieved while providing low sensitivity to supply voltage variations.**

***Index Terms*— Low power, clock signal, non-overlap clock generator, non-overlap period, phase shift.**

I. Introduction

The advancement of VLSI systems stimulated a demand for high performance and low area design implementations. For that reason many novel approaches have arisen as switching capacitor circuits, dynamic and clocked logic gates, which provided high speed with low power dissipation. [1]

NOCGs are common blocks in switched-capacitor (SC) circuits, which provide two non-overlapping clock phases to operate corresponding switches which charge and discharge flying capacitors. [2][3] In order to provide overall low-power performance of the system, NOCGs must meet strict requirements for their own power consumption. Moreover, such characteristics as the non-overlap period (NOP) of dual phase output signals, circuit stability for environmental variations are factors for careful consideration for eliminating problems with clock-skew, signal race, noise and jitter. [4]

II. Structure of Proposed Non-Overlap Clock Generator

For implementation of NOC, NAND/NOR based conventional designs are used which employ a simple chain of inverters to realize delays (Fig.1).[5] These implementations are effective for high frequency clock signals. However, modern SC circuits require lower processing frequencies, thus demanding unacceptable increase in transistor count which results in rise of consumed power and area. Conventional delay elements are sensitive to environmental conditions as supply voltage and temperature variations. To give a solution to mentioned problems a novel structure of NOCG is proposed.

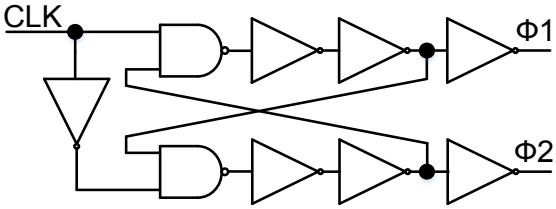

Fig. 1. Conventional non-overlap clock generator

In proposed design three transistor XOR gate has been used (Fig. 2), which consists of two PMOS and one NMOS transistors. [6] When the input B is at logic high, the gate performs like simple inverter. However, when A=1 and B=0, due to threshold drop across M2 transistor, degradation of C output takes place with respect to the input. This configuration is not used in proposed structure.

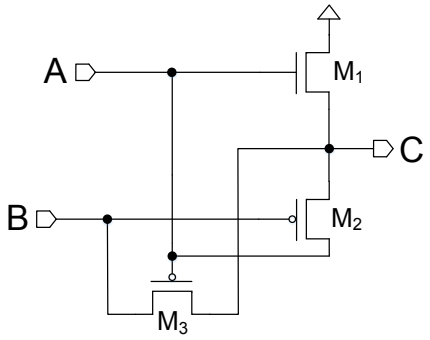

Fig. 2. Three transistor XOR gate

Structure of designed NOCG is shown in Fig. 3. A back-to-back XOR structure is used to generate non-overlap output signal with required NOP. Input clock signal is given to the gates of NMOS pair M9, M11.

In proposed structure a constant high level signal is given to PMOS transistors, which assures OFF state for M2 and M3 transistors. This ensures separation of VDD and ground rails, thus lowering dynamic power consumption. Additionally Vctrl1 is used to control the NOP of output signals, which is another benefit of proposed structure, as in

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conventional NOCGs NOP depends on the count of inverters in delay line which can't be modified without design change. To eliminate shoot-through current from VDD to ground Vctrl1 is set equal to supply voltage of NOCG. This means that output signal bandwidth will depend on the value of supply and Vctrl1voltages.

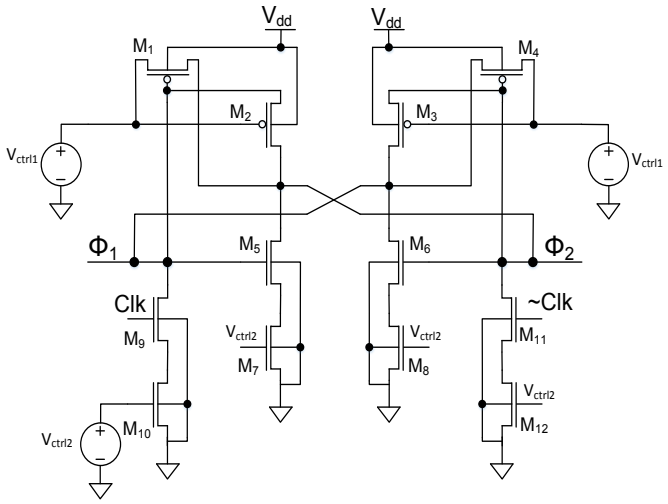

Fig. 3. Proposed non-overlap clock generator

One major downside of three transistor XOR circuit in this configuration is that high level of output signal is driven by input signal. This leads to mismatch of rise/fall times of output signal, as the output node is discharged through ground and charged through control voltage which can vary. To ensure equal rise and fall times and thus to provide 50% duty cycle of output signal, additional NMOS transistors are added in line with M7-M11 to control the discharge current of output node. Additional control voltage is used to adjust bias voltage and therefore the discharge current.

As the output voltage of NOCG can vary depending on the values of control voltages and supply voltage of NOCG itself, additional inverters are used for both output phases to ensure rail-to-rail bandwidth of output signals as well as to increase the driving capability of the circuit. Overall structure of proposed design with load capacitances and input voltage sources is shown in Fig. 4.

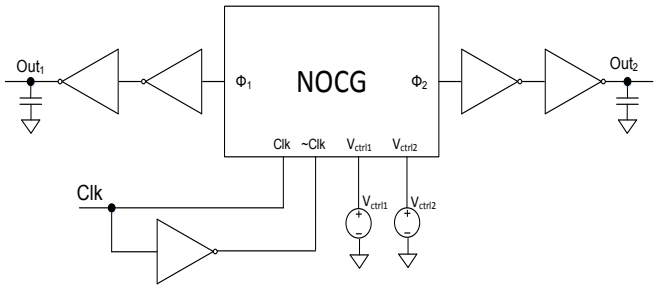

Fig. 4. Simulation circuit of proposed NOCG

III. Simulation Results

Proposed NOCG is designed using CMOS 28nm technology. Fig.5 shows two phase non-overlap output signals of proposed NOCG working with input clock frequency of 70MHz. With 1.2V system power supply and 1V control voltage level a NOP of 185ps is obtained. By adjusting control voltages, NOP is configured from 50ps to 250ps. With conventional NOCG design a delay line of 14 inverters is used to provide 120ps of non-overlap cycle. Which means that proposed design is more efficient in terms of used transistor count, as similar NOP time is obtained using only 20 transistors compared with 64 transistors used in conventional NOCG.

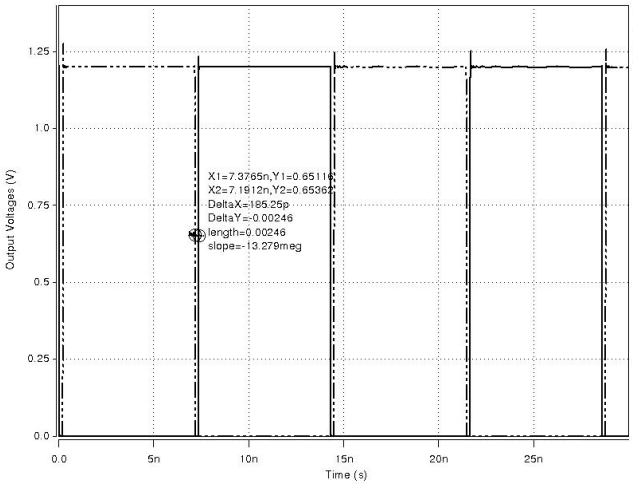

Fig. 5. Two phase output voltages of proposed NOCG

Fig. 6 shows current consumption of both conventional and proposed designs. As mentioned higher, proposed construction doesn't have direct path from VDD to ground, that's why maximal current pulse value reaches up to 100uA for 1V of supply voltage. In case of inverter based NOCG, a shoot-through current is present during input signal rise and fall periods. Moreover, the overall consumed current of NOCG is the summary of all inverters used in the delay line, which leads to consumption of larger currents (reaching up to 0.8mA in described case).

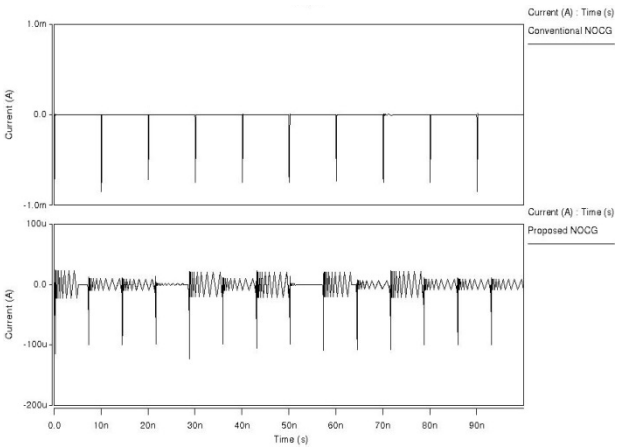

Fig. 6. Consumed currents of proposed and conventional NOCGs

Comparison of dynamic power consumed on one cycle is showed in Fig. 7. Simulation was performed for input clock frequency varying from 20MHz to 500MHz. As the clock frequency increases, the pulse rise/fall times decrease thus lowering shoot-through current for inverter based NOCG. In proposed structure, as shoot-through component of consumed current is much less, it varies less depending on input signal frequency. However proposed NOCG has static current as can be seen in Fig. 6. However, when considering overall consumed power, the proposed structure demonstrates better low-power characteristics.

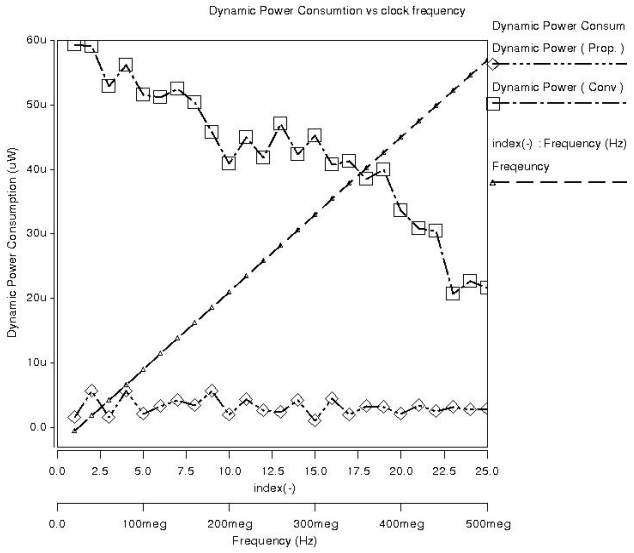

Fig. 7. Dynamic power consumption of proposed and conventional non-overlap clock generators

Another crucial requirement for NOCGs is stability of characteristics towards environmental condition changes as supply voltage. The sensitivity of output signal NOP to variation in supply voltage for proposed design is shown in Fig. 8.

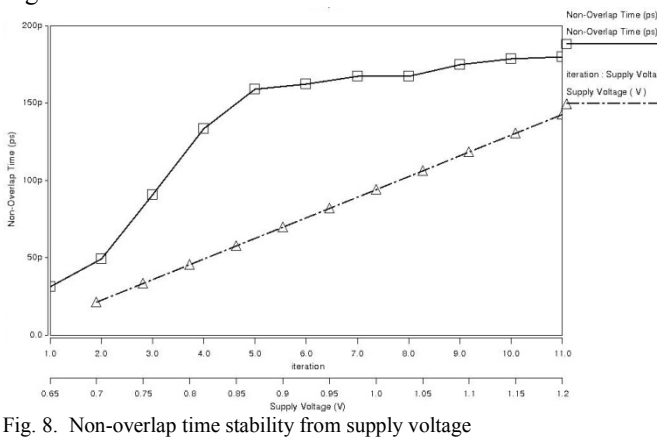

Fig. 8. Non-overlap time stability from supply voltage

As it can be seen from the diagram, NOP is changed from 30ps to 155ps when supply voltage varies from 0.7V to 0.9V, but NOP stays relatively constant for supply voltage change from 0.7V to 1.2V. As the supply voltage in majority of modern low-power systems varies from 0.8V to 1.2V, we can say that proposed structure will provide acceptable deviation of NOP in both multi-voltage applications and in cases of large supply noises.

One of the main sources for uncertainties in SC circuits is the clock signal jitter. Therefore all devices which are located on clock signal generation and distribution path must be designed and optimized to provide low jitter noise and constant duty-cycle of output clock signal.

To examine output jitter level of proposed NOCG, pulse widths of output signals are measured during 300ns time period for 70MHz input clock frequency. As shown in Fig. 9 maximal deviation of pulse widths during simulation period is 16.7ps which is 0.002% from actual pulse width, which is acceptable for most SC circuits.

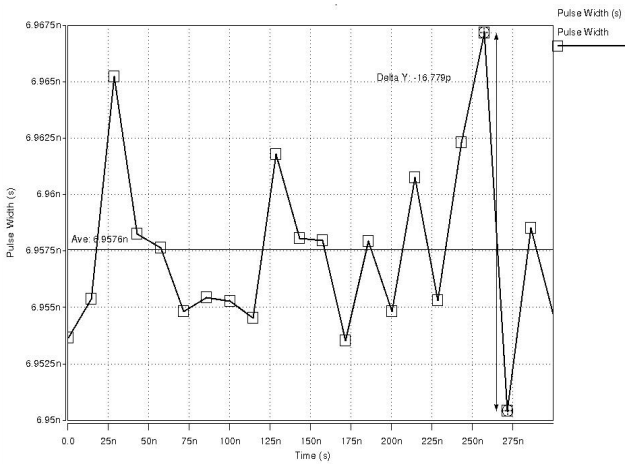

Fig. 9. Output signal jitter measurement

Table 1 shows the performance comparison of proposed NOCG with similar designs. As it can be seen, the proposed structure shows less dynamic power loss, which is the most significant factor of overall power consumption. Moreover, current design is more stable to supply voltage variations.

TABLE I
PERFORMANCE COMPARISON OF THE DESIGNED NOCG WITH SIMILAR DESIGNS IN THE LITERATURE

Parameter	Proposed Design	Conventional Design	[8]
Supply Voltage (V)	0.9-1.2	1.2	1.2
Average Current Consumption (A)	30u	90u	-
Peak Current (A)	110u	0.8m	-
Dynamic Power consumption (uW)	3.5	41.5	3.776
Static Power Consumption(uW)	45	120	34.47
Cload (pF)	5	5	-

Maximal Output Frequency (MHz)	500	900	100
Technology (nm CMOS)	28	28	180

IV. Conclusion

An energy-efficient non-overlap clock generator on three transistor XOR gates is proposed and the respective circuit designed. Designed NOCG provides adjustable non overlap period with fewer number of used transistors while providing acceptable stability and jitter levels around 0.02% of the pulse width. Core structure ensures similar rise and fall times for output signal ensuring 50% duty cycle.

Main drawback of proposed design is the usage to dual variable control voltages. However, taking into consideration that the structure is intended for usage in SC circuits, especially in power converters, multilevel control voltages can be extracted from power converter itself, thus ensuring self-sufficiency of the system.

Acknowledgment

This work was supported by State Committee Science MES RA, in frame of the research project № SCS 13-2I130.

References

[1] R. J. Baker, "CMOS Circuit Design, Layout and Simulation", IEEE Press Series on Microelectronic Systems, 3rd Edition, *2010*

[2] V. Galstyan, V. Melikyan, "Design of low-ripple multi-topology step-down switched capacitor power converter with adaptive control system", Design & Test Symposium (EWDTS), pp. *1-4, 2014*.

[3] V. Zivkovic, P. Petkovic, D. Milovanovic, "Automatic Symbolic Analysis of SC Networks Using a Modified Nodal Approach", Microelectronic Journal, vol. 29, pp. *741-746, 1998*

[4] D. Ma, L. Feng, "Robust multiple-phase switched-capacitor DC_DC power converter with digital interleaving regulation scheme", IEEE Transactions, Very Large Scale Integration (VLSI) Systems, vol 16, *pp. 611-619, 2008.*

[5] H. Milton, F. Catthoor, "A Robust Two-Phase On-Chip Clock Generator", Solid-State Circuits Conference, IEEE, vol. 1, pp. *19-21, 2003*.

[6] S. Singh, T. Sharma, "New design of low power 3T XOR cell" International Journal of Computer Engineering and Technology (IJECT), vol. 3, pp. *76-80, 2012*.

[7] A. Kumar, R. Todani, "Non Overlapping Clock (NOC) Generator for Low Frequency Switched Capacitor Circuits", IEEE, pp. *226-231, 2011*.

[8] O. Prakash, A. Kumar, "Low Power and Area Efficient Implementation of N-Phase Non Overlapping Clock Generator Using GDI Technique", IEEE, pp. *123-127, 2011*.